

CLAIMS

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What is claimed is:

1. A partially fabricated wafer, comprising:
at least one probe pad;
400 multiple test structures which are selectively multiplexed to said probe pad in dependence on the voltage applied thereto.
2. The wafer of Claim 1, wherein said probe pad is located in a scribeline, and occupies more than half the width of said
405 scribeline.
3. The wafer of Claim 1, wherein said multiple test structures are selectively multiplexed to said probe pad in dependence on the voltage applied to said probe pad.
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4. The wafer of Claim 1, wherein said multiple test structures are selectively multiplexed to said probe pad in dependence on the sequence of voltages applied to said probe pad.

415 5. A partially fabricated wafer, comprising:
at least one probe pad;
multiple test structures which are all physically close to said probe
pad, and which are selectively multiplexed to said probe pad
in dependence on at least one global input.

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6. The wafer of Claim 5, wherein said probe pad is located in a
scribeline, and occupies more than half the width of said
scribeline.

425 7. The wafer of Claim 5, wherein said multiple test structures are
selectively multiplexed to said probe pad in dependence on the
voltage applied to said probe pad.

8. The wafer of Claim 5, wherein said multiple test structures are
selectively multiplexed to said probe pad in dependence on the
sequence of voltages applied to said probe pad.

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9. A scribeline test circuit, comprising:

a test selector circuit located in a single scribeline portion between
435 two adjacent die locations;

multiple test structures, also located in said single scribeline portion;
and

at least one probe pad, also located in said single scribeline portion;
wherein said test selector circuit makes an electrical connection
440 from said probe pad only to a selected one of said test
structures, in dependence on the voltage applied at said probe
pad.

10. The circuit of Claim 9, wherein said probe pad occupies more than
445 half the width of said scribeline portion.

11. The circuit of Claim 9, wherein said multiple test structures are
selectively multiplexed to said probe pad in dependence on the
sequence of voltages applied to said probe pad.
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12. A method for testing integrated circuits, comprising the steps of:
(a.) applying a selection signal to a probe pad, to drive a selector
circuit to connect a selected one of multiple test structures to
said paid; and
455 (b.) applying a controlled voltage to said pad, and thereby
measuring the electrical characteristics of the selected one of

said multiple test structures.

TEXAS INSTRUMENTS

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